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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,239	08/07/2001	Edward Tang Kwai Ma	20661-00788	2767

7590 05/26/2004

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 05/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,239	MA ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10,16-28 and 34-38* is/are allowed.

6)☐ Claim(s) *11-15 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-10, 16-28, 34-38 are allowed.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harthcock (U.S. Patent number 6347368).

4. As per claim 11, He teaches (col. 2, lines 25-27) apparatus and method for data exchange with microcomputing devices. He also teaches a first bus, a primary instruction bus from which the device core receives application instructions, a secondary bus which the device core receives

data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle. He thus teaches limitations pertain to assigning a first memory to a first logical locations, and assigning a second memory to a second logical location, since he teaches a primary instruction bus from which device receives application instructions, therefore would include a first memory and a second memory assigned with the secondary bus. He does not explicitly disclose adjusting a memory indicator that causes a utilization of the first memory for a second operation and the second memory for the first operation. He teaches as stated above core receiving data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that He clearly provides the capability to utilize the first memory for a second operation and the second memory for the first operation, since He provides data exchange instructions and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, thereby provides the capability as claimed.

5. As per claim 12, He teaches as stated above device core receives data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, therefore would include a register with a bit indicating a memory indicator.

6. As per claim 13, He teaches as stated above core receiving data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the

instruction buses the core fetches instructions on any given cycle, therefore the operation includes an instruction code access.

7. As per claim 14, He also teaches (col. 2, lines 39-41) added instructions that allow the device to perform data exchange instructions such as read and write with a single word data exchange instruction. He thus teaches instructions for a data access.

8. As per claim 15, He teaches (col. 2, lines 34-38) a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, therefore would include circuitry to actuate a system reset, since he teaches circuitry for selecting from which of the instruction buses the core fetches instructions, and furthermore, he teaches a microcomputing device, which is well known in the art to provide a system reset capability.

9. Claims 29-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harthcock (U.S. Patent number 6347368).

10. As per claim 29, Harthcock substantially teaches the claimed invention as disclosed related to claim 11 above. He also teaches (col. 2, lines 25-27) a first bus, a primary instruction bus from which the device core receives application instructions, a secondary bus which the device core receives data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle. He thus teaches limitations pertain to assigning a first memory to a first logical locations, and assigning a second memory to a second logical location, since he teaches a primary instruction bus from which device receives application instructions, therefore would include a first memory and a second memory assigned with the secondary bus. He does

not explicitly disclose means for adjusting a memory indicator that causes a utilization of the first memory for a second operation and the second memory for the first operation. He teaches as stated above core receiving data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle. It would have been obvious to a person of ordinary skill in the art to realize that He clearly provides the capability to utilize the first memory for a second operation and the second memory for the first operation, since He provides data exchange instructions and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, thereby provides the capability as claimed.

11. As per claim 30, He also teaches (col. 2, lines 39-41) added instructions that allow the device to perform data exchange instructions such as read and write with a single word data exchange instruction. He thus provides the capability to utilize flash memories for the first and second memories.

12. As per claim 31, He teaches as stated above device core receives data exchange instructions, a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, therefore would include a register with a bit indicating a memory indicator, and would utilize a nonvolatile memory since he teaches to perform instructions such as read and write with a single word data exchange instruction.

13. As per claim 32, He teaches (col. 2, lines 34-38) a circuitry for receiving data exchange instructions, and circuitry for selecting from which of the instruction buses the core fetches instructions on any given cycle, therefore would include circuitry to reset the memory indicator,

since he teaches circuitry for selecting from which of the instruction buses the core fetches instructions, and furthermore, he teaches a microcomputing device, which is well known in the art to provide a system reset capability.

14. As per claim 33, He also teaches (col. 2, lines 39-41) added instructions that allow the device to perform data exchange instructions such as read and write with a single word data exchange instruction. He thus provides means for resetting the first and second memories.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (703)-308-5228. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703)-305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114